The Electronics and Data Acquisition Systems for the BESS-Polar Program

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***Abstract*. The Balloon-borne Experiment with a Superconducting Spectrometer, BESS, has been carried out to study elementary particle phenomena in the early Universe through cosmic-ray observation, including measurement of low energy antiprotons to investigate their origin and search for antihelium. The BESS-Polar is an evolutionary development of the BESS program to study these topics much further by using long-duration balloon flights over Antarctica. The front-end electronics and data acquisition systems of BESS-Polar were newly developed to adapt to severe requirements of the Antarctica flight. The low-power front-end-electronics, using techniques originally developed for space instruments at Goddard Space Flight Center, achieved a total power consumption of less than 450 W, which is close to one third of the power consumption of the previous BESS experiments. The high speed data acquisition system using USB2.0 interfaces and CompactPCI embedded computing system achieved full data processing and recording with dead time 23% under the condition of 3 kBytes typical event size and 3.4 kHz event rate in Solar minimum. These systems were flown nearly 38 days above Antarctica, successfully recording 5.5 billion events in the two BESS-Polar flights.**

***Keywords*: BESS-Polar, Front-End-Electronics, Data acquisition**

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I. Introduction

The Balloon-borne Experiment with a Superconducting Spectrometer, BESS, is part of a US-Japan cooperative balloon program in the field of particle astrophysics that aims to study elementary particle/antiparticle phenomena in the early history of the Universe[1], [2], [3]. To study the topics with much higher statistics, the long-duration balloon flight over Antarctica (BESS-Polar) was carried out twice in the austral summer season of 2004-2005 (BESS-Polar I) and 2007-2008 (BESS-Polar II). The detector systems of the BESS-Polar experiment are evolutionary developments of those used in the previous BESS experiments[4], and improved to adapt to a long duration flight in Antarctica. The outer pressure vessel was eliminated to minimize the materials which incident particles pass through, consequently the Time-of-Flight Counter (TOF)[5] and Aerogel Cherenkov Counter (ACC)[6] and related front-end electronics were exposed to ambient condition during flight. The solar power system was used to reduce the weight and provide stable power for more than 20 days with a capacity of 900 W. The trigger rate varied depending on the solar activity from 1.5kHz to 2.5kHz and typical event data size was about 2 kBytes.

The electronics and Data Acquisition (DAQ) systems were newly developed to adapt those conditions. For the BESS experiment, standard CAMAC and VME systems were used for the DAQ system. Since the DAQ system in the previous BESS experiment was not fast enough to process all data with an acceptable dead time, an intelligent second-level trigger system was introduced to remove the overwhelming positive charged CR background in the antimatter search. For the BESS-Polar flight, instead of using any standard bus format, each modules were controlled through a serial interface, USB

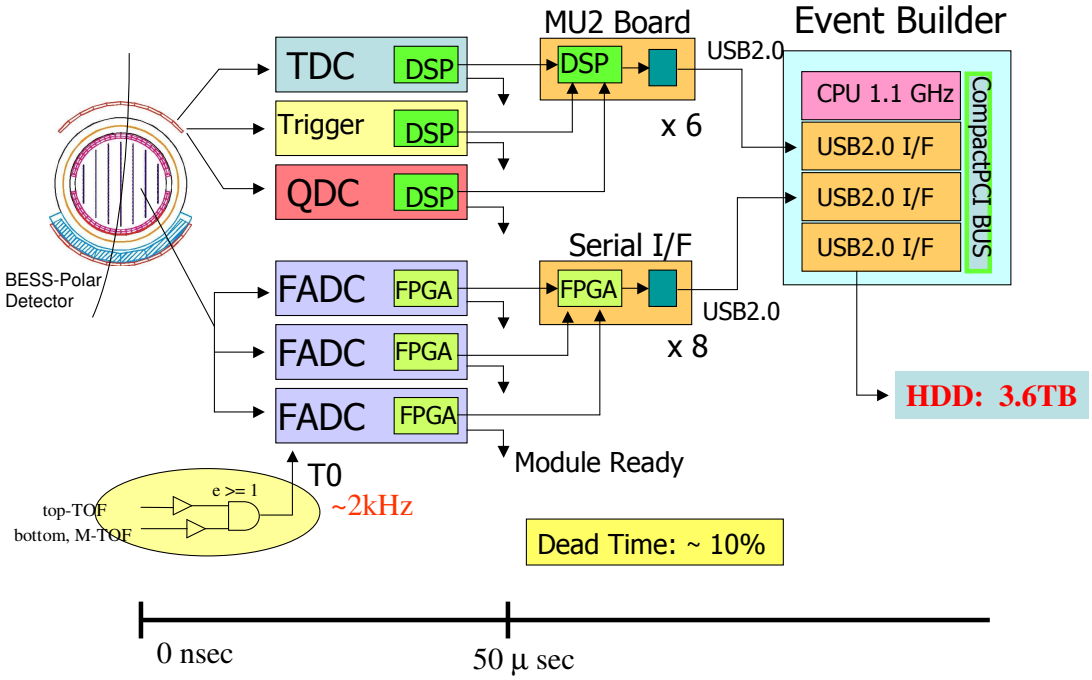

Fig. 1. A block diagram of the BESS-Polar I DAQ system. For the BESS-Polar II, new CPU board with Core Duo 1.66 GHz was used and HDD capacity increased to 16 TBytes. Also, each FADC had the Serial I/F.

2.0. A high performance and low power consumption CPU allowed us to process the all data without any onboard event selection, so that the trigger system could be simplified and reduced the total power consumption. Also low-power front-end electronics were developed employing techniques originally conceived for space instruments at Goddard Space Flight Center.

II. System Overview

Figure 1 shows a block diagram of the BESS-Polar DAQ system. The signals from the detector are digitized by the dedicated Front-End Electronics (FEEs) then send the digitized data to the event builder through USB 2.0 signal. The signal from the outer and middle TOF and Aerogel Cherenkov are digitized by the time-to-digital converter (TDC) boards and the charge-to digital converter (QDC) boards. The signals from the drift chamber are digitized by the flashADC (FADC) boards. The T0 trigger is generated by the trigger board with the coincidence of hits in the top and either the bottom or middle TOF counters. The trigger board sends the trigger signal together with an 8-bits event number to each FEEs to initiate the digitization. The event number is used for the event building process. Once T0 trigger is generated, the trigger board is locked until the trigger board receives a "Ready" signal from all FEEs. To minimize the dead time caused by the event processing, each FEE sends the "Ready" signal to the trigger board independently just after it finishes digitization. The dead time can be kept under 10% if each of the FEEs finishes this process within 50 microseconds. The data from each FEEs are sent to the CompactPCI (cPCI) embedded system individually together with the event number which was received from the trigger board, then recorded to the HDDs after building the event of a given event number. In order to prepare for the higher trigger rate expected for the BESS-Polar II flight conducted at Solar minimum, each FADC module had a dedicated serial interface so that data throughput rate could be maximized. And at the same time, the CPU board was upgraded to a Core Duo 1.66GHz and the capacity of data storage increased to 16 TBytes.

III. The Front-End Electronics

The time-to-digital converter (TDC) boards incorporate fast discriminators and common-stop time digitizers to detect signals from the three TOF layers (top, middle and bottom) and measure their arrival times. The output pulses from the discriminators are also fed into the trigger. The TDCs have a full range of 150 nanoseconds and a resolution of better than 43 picoseconds for measured times up to 100 nanoseconds. For the top and bottom TOF, PMT anodes are coupled directly to the TDCs. For the middle TOF, the dynode signals are coupled to the TDC through an inverting amplifier with a gain of ten and a bandwidth of more than 1 GHz.

The charge-to-digital converter (QDC) measures the integral charge of PMT signals from the ACC, outer TOF and middle TOF. The QDCs can be set to measure negative charge pulses from the PMT anodes (ACC and middle TOF) or positive pulses from the PMT dynodes (TOF). The full-scale ranges of the QDCs is tailored to match the needs of individual detectors and are set at

250 picocoulombs for the ACC, 1000 picocoulombs for the outer TOF, and 2000 picocoulombs for the middle TOF. Sixteen bit digitizers are used and in bench tests using a precision charge pulser, the QDCs have demonstrated a good linearity and a resolution of better than two bits (LSB). With a PMT of flight event rate, the effective dynamic range is 12 bits mostly due to a recharge time constant of the PMT base. The power consumption of the QDC is about 0.16 W per channel. It corresponds to 1/2 of the previous BESS QDC.

The trigger board receives the discriminator outputs from the TDC boards, generates a T0 trigger based on a programmable coincidence and distributes the T0 trigger to all FEEs. Also a periodic T0 trigger is issued by an internal clock to evaluate the FEEs performance during the flight. Since FEEs send the data to the event builder independently, the trigger board distributes an 8-bit event number in order to synchronize each data segment of an event in the FEEs. A scaler on the trigger board counts the discriminator outputs from each channel on the TDC boards. These scaler values are sent as monitor data to the ground in every 15 seconds. Any noisy PMTs can be removed from the coincidence pattern by command from the ground.

The flash-ADC (FADC) board measures the charge signal from the drift chamber wires at 512 sampling points from the T0 trigger. The sampling rate is 32 MHz and chosen to cover the full drift time of the drift chambers. Since the raw data from the FADC board are too large to be processed in appropriate time, a compression method is employed to reduce the data size. The compression reduces the data size to 64 bits per hit channel (See Figure 2 and Table I). The power consumption of the FADC is about 0.14 W per channel.

TABLE I
VARIABLES OF THE COMPRESSION DATA AND THEIR DATA SIZE.

Type	Name	Data Size
Packhet Header	Header	4 bits
Time between T0 to 1st Data	Time	10 bits
FADC value for the 1st Data	1st Data	10 bits
FADC value for the 2nd Data	2nd Dta	10 bits
Width of the pulse	Width	10 bits
Total Charge	Charge	16 bits
Over flow flag	Flag	4 bits
Total	–	64 bits

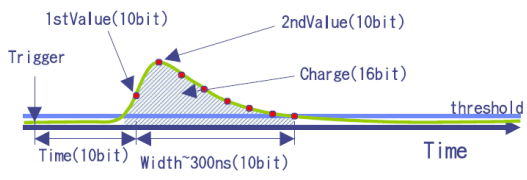

Fig. 2. A schematic view of drift chamber signal and FADC compression value.

IV. The Data Acquisition System

The hardware of the Data Acquisition (DAQ) system consists of a commercial CPU board and USB 2.0 Interface cards. The form factor is the cPCI and the crate was mounted in an pressurized ion vessel serving as magnetic shielding to operate in high magnetic field. The software of the DAQ system was developed with C++ code using the ROOT[7] library run on a Linux operating system. The OS was installed on a Compact Flash. For the BESS-Polar I flight, the Slackware 9, kernel 2.4 was used. For the BESS-Polar II flight, the Scientific Linux 5 with kernel 2.6 was used.

For the FEEs of TOF and ACC, a Digital Signal Processor (TMS320VC5402 [8], Texas Instruments) is resident on each board and controls each board independently to maximize the data throughput rate. The event-builder subsystem board (MU2 board) acts as a mediator between the FEEs and the cPCI embedded system. Up to three FEEs are connected to one MU2 board through Multichannel Buffered Serial Ports (McBSPs), then connected to the cPCI embedded system through USB 2.0. Figure 3 shows the block diagram of the TDC board's digital section. The program for the DSP is burned onto a FLASH ROM (28F160B3, Intel) using the DSP emulator (XD510 USB JTAG Emulator, Spectrum Digital, Inc.) through a JTAG port. The DSP is booted at power-on time by reading the program from the FLASH ROM and initializing the board [10]. The data digitized at the analog section is read by the DSP through the FPGA (EPM7256AET, ALTERA). The DSP packs the data of 12 channels and sends them to the MU2 board. The event processing time for one event is about 30 microseconds. The data from up to three FEEs board are gathered in the MU2 board and converted to a USB 2.0 signal using a USB Microcontroller (EZ-USB FX2 CY7C68013 [9], Cypress).

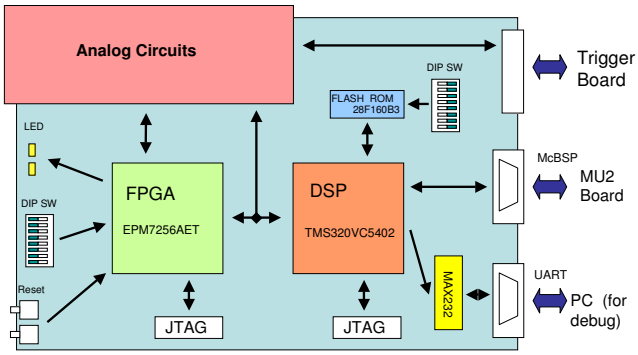

Fig. 3. A block diagram of the BESS-Polar TDC board.

For the FEEs of JET and IDC, two FPGA are resident on each board. One FPGA (EP20K400EBC652-3, ALTERA) dedicated to the data compression of the FADC raw data and the other FPGA (EP20K300EQC208-2X, ALTERA) used to

communicate with a USB Microcontroller. For the BESS-Polar I flight, the data from three FADC board gathered into one FADC board then converted to a USB 2.0 signal. For the BESS-Polar II flight, each FADC board had the USB Microcontroller to accommodate higher trigger rate expected during a flight in Solar minimum. Due to this modification, the total number of the USB Microcontroller became grater than 16, which exceed the maximum number of connectable USB module to the linux kernel for one kind of USB device. In order to avoid this limitation, two different Vender ID and product ID were assigned to the USB Microcontroller, so linux recognize there are two different usb devices both of which connected less equal 16.

V. The Control and Monitor System

During the flights, the spectrometer was controlled and monitored from ground through telemetries. Figure 4 shows a block diagram of the communication flow. The PC104 system was used both at ground and on payload. By connecting the ground PC to the PC104 flight system through ethernet, a same operation condition except telemetry communication could be provided during ground test.

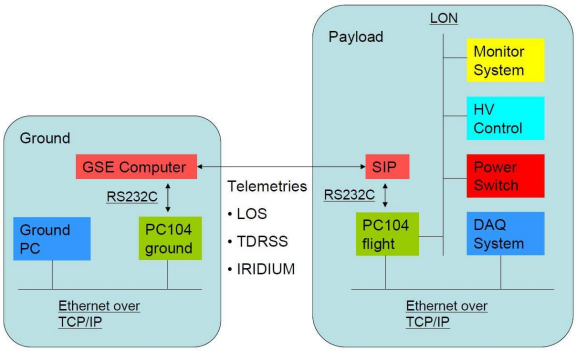

Fig. 4. A block diagram of the BESS-Polar communication flow.

The PC104 system consists of CPU (Kontron, MOPSIcdGX1, 300MHz) board, LON (Local Operating Networks) board, and telemetry boards. The Linux (Slackware 9.1, kernel 2.4) was employed as the OS and installed on the chipdisk (Kontron, chipDISK 128MB). The power switch control boards, high voltage control boards and monitor boards were connected to the PC104 system through LON by twisted pair cables. The DAQ system were connected to the PC104 system through ethernet over TCP/IP.

VI. Summary

The low power consumption FEEs and fast DAQ system was newly developed for the BESS-Polar program. Using techniques originally developed for space instruments at Goddard Space Flight Center, achieved a total power consumption of less than 450 W, which is close to one third of the power consumption of the previous BESS experiments. The high speed data acquisition system using USB2.0 interfaces and CompactPCI embedded computing system achieved full data processing and recording with dead time 23% under the condition of 3 kBytes typical event size and 3.4 kHz event rate in Solar minimum. These systems were flown nearly 38 days above Antarctica, successfully recording 5.5 billion events in the two BESS-Polar flights. Table II compares the key parameters of the BESS, BESS-Polar I and BESS-Polar II.

TABLE II
Comparison of BESS-Polar II with BESS-Polar I and BESS

	BESS(1997)	BESS-Polar I	BESS-Polar II
Geometrical acceptance	$0.3m^2str$	$0.2m^2str$ effective	$0.3m^2str$
Data storage	120 GB	3.6 TB	16 TB
Trigger rate	2.1 kHz	1.4 kHz	3.4 kHz
Data acquisition rate	0.3 kHz	1.2 kHz	2.5 kHz
Dead Time	12 %	20 %	23%
Flight Duration	1 day	8.5 day	24.5 days magnet on
Power Consumption	1.2 kW battery	450 W solar panel	450 W solar panel

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