The analog readout system of the RPCs in the ARGO-YBJ experiment

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***Abstract*. The ARGO-YBJ experiment is in stable data taking since November 2007 at the YangBaJing Cosmic Ray Observatory (Tibet, P.R. China, 4300 m a.s.l.). It is an air shower detector able to operate with an energy threshold of a few hundred TeV, consisting of a single layer of RPCs operated in streamer mode, covering a total instrumented area of about 11,000 $\mathbf{m^2}$. Signals from each RPC are picked up with 80 readout strips 61.8 cm long and 6.75 cm wide. By counting the number of secondary particles, the strip readout allows the measurement of energies up to a few hundred TeV. In order to extend the dynamic range to PeV energies, an analog readout has been implemented by instrumenting each RPC with two large size pads of dimensions 1.25×1.40 $\mathbf{m^2}$. In this paper we describe the charge readout system of the ARGO-YBJ experiment.**

***Keywords*: Cosmic Rays, RPC analog readout**

I. INTRODUCTION

The ARGO detector is constituted by a central carpet ∼78×74 m^2, made of a single layer of Resistive Plate Chambers (RPCs) with ∼93% of active area, enclosed by a guard ring partially (∼20%) instrumented up to ∼110×100 m^2. The apparatus has a modular structure, the basic data acquisition unit being a Cluster (7.6×5.7 m^2), made by 12 RPCs (1.25×2.8 m^2 each). Each chamber is read out by 80 strips of 61.8×6.75 cm^2 (the spatial pixels), logically organized in 10 independent pads of 61.8×55.6 cm^2 which correspond to the OR of 8 contiguous strips and represent the sampling unit of the particle arrival time (time pixel). The full detector has 153 clusters with a total active surface of ∼6700 m^2 [1].

The digital signals coming from the front-end electronics are processed by the Receiver cards housed inside the Local Station (LS) crate[2]. Each Receiver card collects the signals coming from a chamber, in such a way that adjacent strips are logically OR-ed (Fast-OR) together in groups of 8, the logic pad, that is sampled by a digital multi-hit TDC with a time resolution of about 1 ns. The high granularity of the detector and its time resolution provide a detailed three-dimensional reconstruction of the shower front.

The LS crate manages and contains 12 Receiver cards, one IN/OUT card for the communication with the Data Acquisition System (DAQ) and one active backplane. The LS provides the fired pad multiplicity of a Cluster to a Trigger System which generates the experiment trigger when the number of the fired pads in the central carpet exceeds a programmed threshold[3] within a coincidence window of $\sim 400\ ns$.

The trigger signal is sent to each LS where it acts as a common stop for all the TDCs, then the TDC counts and the pattern of the fired strips are collected and transmitted to the central DAQ.

Since we have a strip density of about $23/m^2$, this implies a saturation in the energy estimate at about a few hundred TeV depending on the primary particle. In order to reach PeV energies, particle densities larger than $10^3/m^2$ have to be measured. In order to this, the signal readout of two large size pads, 1.25×1.40 m^2, the so-called Big Pads (BP), on each RPC has been implemented.

A single particle pulse on the BP, with RPCs operated at sea level at 9.5 kV, with a gas mixture made of 15% Ar, 10% Isobutane and 75% R143a, has a rise time in the range of about a few tens of ns, a constant discharge time of many μs and an amplitude, on a 50 Ω load, of about 2 mV, but the BP signal can be as high as many Volts [4].

II. THE CHARGE READOUT SYSTEM

The BP signals of two adjacent Clusters are processed by electronic modules hosted in a custom crate, called MINICRATE, that has two independent sections, each one containing 3 readout cards (CHargeMeter cards) and a Control Module. The CHargeMeter (CHM) processes 8 analog signals and digitizes them, while the Control Module builds the local data frame of 3 CHM boards and transfers it to the Local Station, which finally provides the data to the central DAQ. A simplified logic scheme of a MINICRATE section is shown in fig. 1.

A 5 m coaxial cable is used to feed the signal to the CHM input adapted to 50 Ohms. The CHM board is

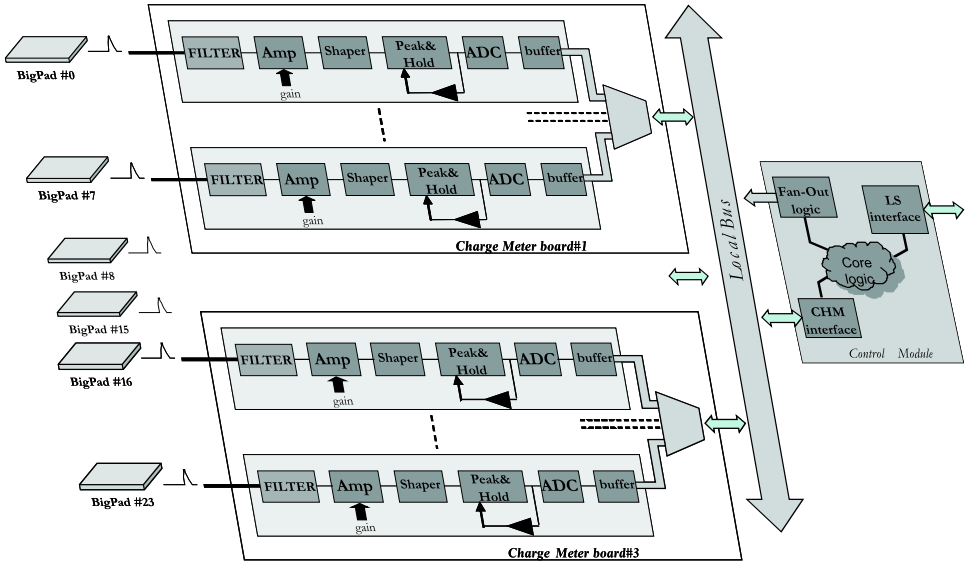

Fig. 1: The logic block diagram of one MINICRATE section

made of 8 identical sections. The first block of each section consists of a voltage filter able to cut out spikes greater than 40 V to protect the next electronic stages. It follows a linear amplifier with a dynamic gain set by a 3-bit programmable register, which provides 8 full scale values, namely 0.33, 0.66, 1.3, 2.5, 5, 10, 20 and 40 V. Operating the system at different scales allows an overlap between digital and analog readout which is an efficient way to calibrate the analog system. In the next step the long tail of the BP signal is cut out by doubling and inverting the signal, then summing the original to the inverted one with a Δt delay. This time delay has been set to $\sim 500\ ns$ to guarantee that the analog signal reaches its maximum and to be sensitive to delayed particles in the shower front. A Peak and Hold (P&H) circuit represents the core of the next stage. It continually samples the output of the previous stage and keeps the highest reached value for 2 μs; the tilt time of the P&H is 4mV/μs, which does not cause any trouble with respect to the trigger jitter time as already shown in [4]. After 2 μs the P&H is reset and then it starts again to sample the signal from the previous stage. If a conversion signal arrives, the ADC starts to digitize the P&H amplitude and keeps the digitized data. The conversion signal is generated by the LS when the local multiplicity, fired pads in the Cluster, gets higher than a programmable threshold, namely $\geq 16, \geq 32$ and ≥ 64. The ADC data collection is managed in each section by the Control Module via a custom bus protocol operated on the backplane lines. The Control Module receives a local density trigger from the LS and distributes it to the 3 CHM units starting the ADC digitalization. Then, each CHM board replies by asserting a local Busy signal in order to prevent the generation of further local triggers so to guarantee the correct ADC conversion. After 14 clock cycles at 10 MHz the data are converted, within 135 ns they are leatched and ready to be sent by the Control Module to the FIFO of a special Receiver board of the LS. The transfer to the FIFO occurs only if the experiment trigger confirms the local one; actually the Control Module is equipped with a time-out counter set at 1.6 μs (count-down timer). This timer starts when a local trigger occurs and stops when a main trigger (Common Stop) arrives from the Trigger System. If this counter is greater than zero, the local trigger is validated and the data stored in the ADCs are transferred to the FIFO, otherwise the data will be discarded and the ADC system will be ready to process a new local trigger. The Busy signal is reset either after data transfer or when the counter gets to zero. A multiplexer logic provides a simple and flexible data readout. Each CHM board readout is performed in 4 clock cycles (400 ns) by merging two words and the whole section is processed in 1.2 μs.

The Control Module takes care of: a) data reading from 24 ADCs according to a fixed protocol and their transfer to the LS; b) calibration of each electronic channel in order to keep linearity and stability of the system under control; c) setting up of the amplification gain for each electronic channel; d) selection of the local multiplicity to be used as a trigger.

The board consists of two sections: one manages the ADC boards in clock and trigger distribution, readout and data transfer; the other section (setting up) takes care of the communication with the central DAQ for set-up and ADC board calibration . Each section is implemented in a Spartan Xilinx FPGA. A PLD of the 9500 family is used in addressing-enabling ADC boards. The second section has a two-way serial bidirectional communication line at the speed of 1 Mbit/s.

III. The analog data transfer

The integration of the BP data in the main data flow has been done by adding one virtual pad, numbered

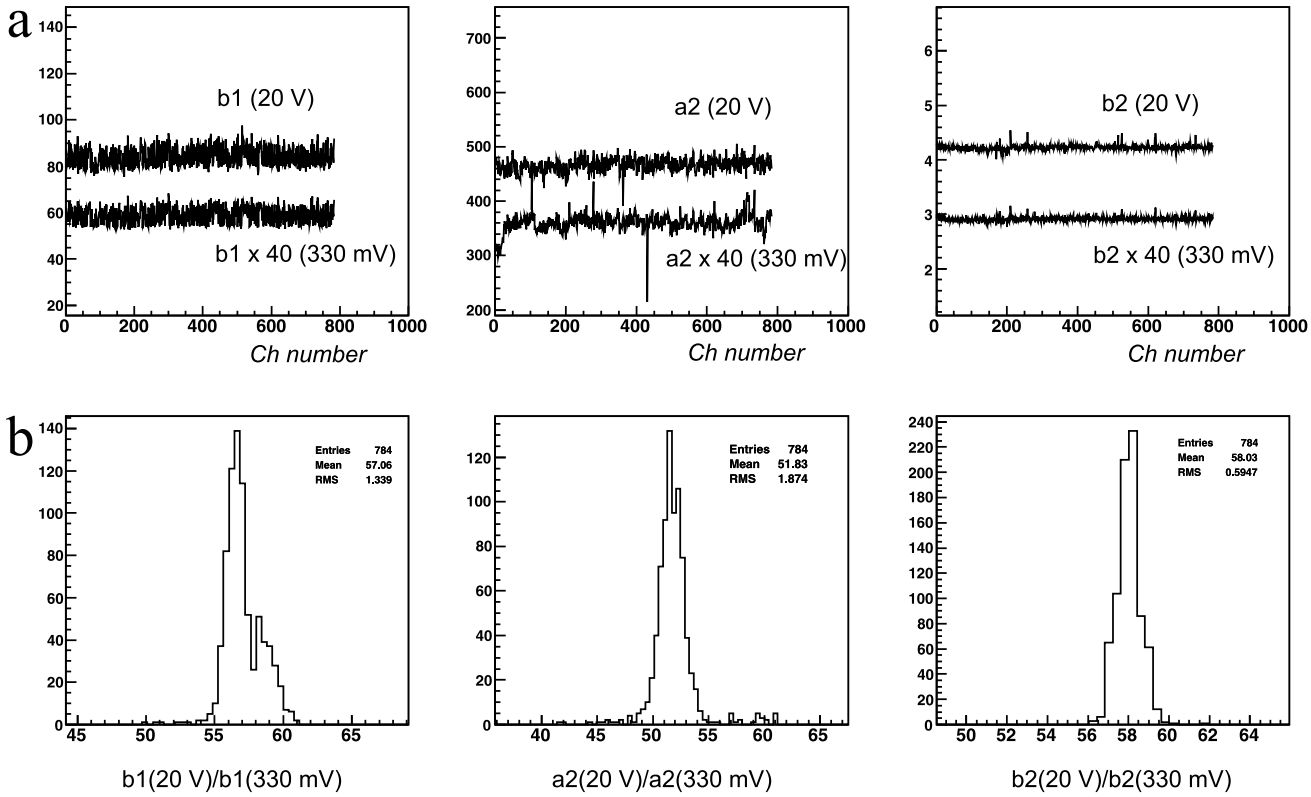

Fig. 2: a) behaviour of the b_1, a_2, b_2 parameters (see text for explanation) for two reference scales, 0-330 mV and 0-20 V; b) ratio of the parameters values in the two reference scales.

as 121, to the 120 pads of each LS. Thus, the ADC data are stored like a strip pattern coming from the pad 121. In order to collect the information of pad 121, a special Receiver board of the LS has been provided with a FIFO realized with a Spartan Xilinx FPGA. The depth of the FIFO is 50 bytes (48 ADC data + 2 control words) because each ADC word (12 bits) is split in two 8-bit words. The FIFO has been implemented with a Dual Port Memory in order to have two independent read/write buses. The FIFO can be read while the Control Module is filling it, provided, the writing is faster than the reading. Finallay, the data frames stored both in the standard Receivers and in the modified one are transferred to the central DAQ.

IV. Test results

At present, the system is going to be assembled at YBJ in its final form; we have already operated a preliminary version of the analog readout on a few Clusters since December 2004[5]. Here we report on the results of a few major tests that have been done in order to understand the performance, the homogeneity of the board production, the homogeneity of the electronic channels, linearity and calibration features. Test results have already been reported in [4][5]. The calibration is certainly crucial for the analog system, so we tried different ways[5][6] to calibrate our CHM boards. First, an external system able to generate pulses up to 10 V and read the ADCs has been set up with an ORTEC generator; pulses where generated with a 10 mV step. The functional form that has been used to correlated ADC count and pulse amplitude A is:

$$A = \begin{cases} a_1 + b_1\sqrt{ADC_{count}} & 0 < ADC_{count} < 200 \\ a_2 + b_2 \cdot ADC_{count} & 200 < ADC_{count} < 4096 \end{cases} \quad (1)$$

The behaviour of the parameters b_1, a_2 and b_2 as a function of the channel number is shown in fig. 2a for a sample of about 100 CHM boards of 800 electronic channels in the two scales 0-330 mV and 0-20 V. The parameters in both scales follow the same behaviour as confirmed in fig. 2b, where the ratios of the parameter values in the two scales are reported.

We repeated the same analysis for each positional channel in the board, say all channels #1,#2,..#7, and we verified that the position in the board does not imply any substantial difference in the channel behaviour as shown in fig. 3 for parameter b_2; only the channel #4 shows a little different mean value with respect to the other channels, but within 1 RMS. The calibration procedure has been repeated by using a full MINICRATE electronics, where pulses were generated by the DAC of the Control Module; in fig. 4 we show the calibration data of one channel in the V_{in} range 0-2.5 V. A linear fit has

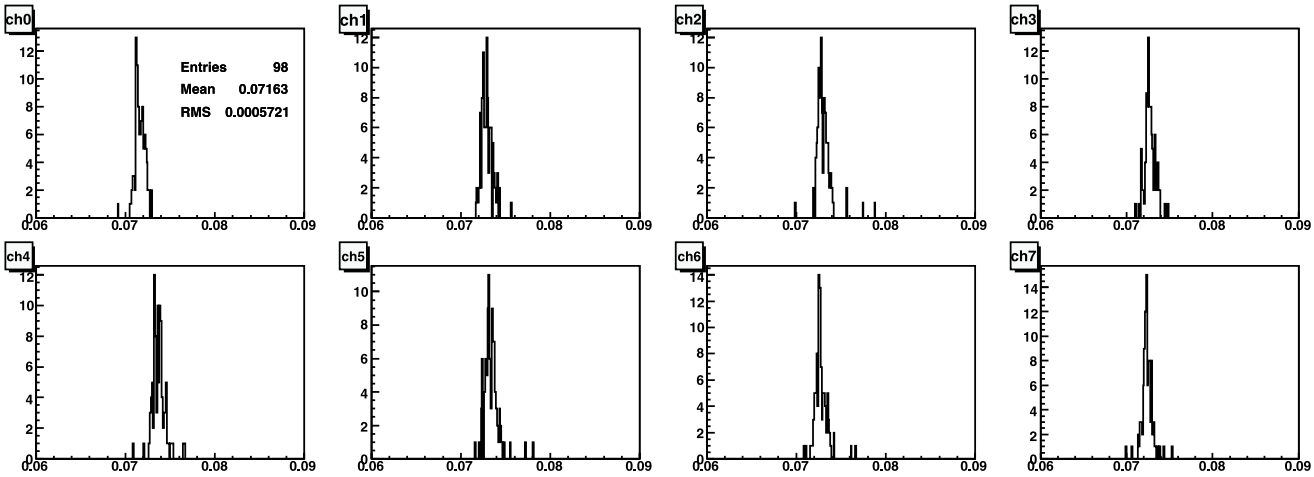

Fig. 3: distribution of the b_2 parameter for different positional channel (0-7) in the CHM board.

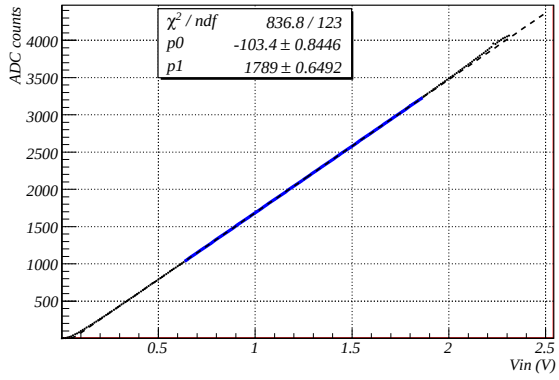

Fig. 4: single channel calibration: typical ADC count vs V_{in} for one channel

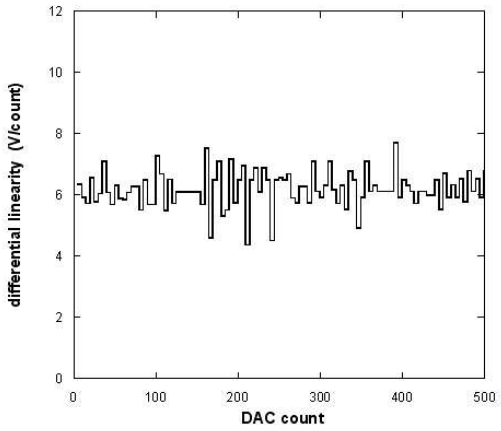

Fig. 5: differential linearity of DAC pulse generated in the Control Module

been performed in the central part of the input voltage range, as put in evidence by the heavy line, while the extrapolation to the upper and lower part is in dashed line. The integral linearity in the upper parts is about 1%, as well as in the lower part of the scale provided that the first 5% of the scale range is excluded; this conclusion is independent of the full scale setting. The distribution of the parameters shown in fig. 2 and fig. 3 are the same. The DAC differential linearity, measured with a LECROY 454 oscilloscope (500 MHz, 2GS/s) is reported in fig. 5, where it can be seen that the DAC provides a signal whose increase is exactly 6.1 mV/count, apart from the first bin.

V. Conclusions

The analog readout system of ARGO-YBJ will be fully operating within a few months. Test results confirm the design expectations, or the ARGO capability to operate at very high particle density ($> 10^3/m^2$). We expect that operating the ARGO detector at PeV energies along with the specific features of the apparatus, particularly the full coverage, will open a new window on cosmic ray physics.

VI. Acknowledgements

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