Development of a gigahertz-sampling analog memory ASIC for an imaging atmospheric Cherenkov telescope

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***Abstract*. High speed waveform sampling has been required for an imaging atmospheric Cherenkov telescope to reduce the effect of the night sky background. We have developed the waveform sample ASIC called Analog Memory Cell (AMC) with a high speed sampling frequency of around 1G Hz, fabricated in 0.5 μm CMOS process. The latest version of AMC has an input channel consisting of 64 capacitors which correspond to the sampling depth of 64 nsec. We digitalize the charge of each capacitor by using a slow (30 MHz) but high resolution (12 bit) ADC. The AMC has a dynamic range of more than 10 bit and an integrated non-linearity of less than 0.4 %. We have been developing the next version of the AMC with 256 capacitors and will report the current status.**

***Keywords*: ASIC, Analog memory, Analog to digital conversion**

I. Introduction

Ground based imaging atmospheric Cherenkov telescopes (IACTs) observe Cherenkov light from an extended air-shower. Night Sky Background (NSB) is a major noise for IACTs. NSB comes from all region of the sky to the pixel photon detector of IACT with very high frequency of 10-100 MHz and its typical amount known as Jelly's values [4] is 6.4×10^7 photons/cm^2/str/sec (4300–5500 Å). Since the detected NSB is proportional to the signal integration time, it is needed to shorten the integration time as possible to improve the signal-to-noise ratio. This feature requires an analog-to-digital converter (ADC) to convert a signal at a sampling frequency of $\sim$ 1 GHz, because the time constant of the Cherenkov light from the EAS is less than 10 ns. An IACT has a thousand pixel photon detectors and requires a dynamic range of more than 10 bit. Low power consumption, a cheaper price, and a compactness of a module are also required. The ADC which satisfies requirements of a high speed and a wide dynamic range is a commercial flash ADC. The flash ADC, however, consumes a relatively high power of a few W per channel at a high cost. Another method to digitalize the signal is needed.

We are developing an Analog Memory Cell (AMC) for IACTs [1]. This is a type of a switched capacitor array (SCA) and can sample the signal with a high speed and wide dynamic range. Some SCAs have been developed for IACTs such as SAM for H,.E.S.S.-II and DRS for MAGIC-II [2] [3]. The AMC has originally been developed for sampling a fast signal from Cherenkov ring detector such as a photo-multiplier tube (PMT) or a Hybrid Avalanche Photo-Detector (HAPD). The AMC can sample a waveform with a high speed of 1 GHz. The AMC is an ASIC fabricated in 0.5 μm CMOS technology. By using CMOS technology, the AMC consumes less power, and its entire circuit is very small. Typical electric power is less than 100 mW per channel with a supply voltage of 0–5 V, and its area is 16 mm^2. Figs. 1 and 2 show the photograph and the schematic view of the AMC, respectively.. A capacitor is switched off when a trigger signal is inputted to the switch. By delaying this trigger signal by a delay line, each capacitor has an electric charge which reflects an input signal level at the switch-off timing in sequence. By reading the charge stored in each capacitor, we can reconstruct the waveform of the input signal. Delay time through each delay buffer is 1 ns. This value directly corresponds to the sampling frequency of 1 GHz. Some modifications in this delay line are going to be done to improve the accuracy of the delay time.

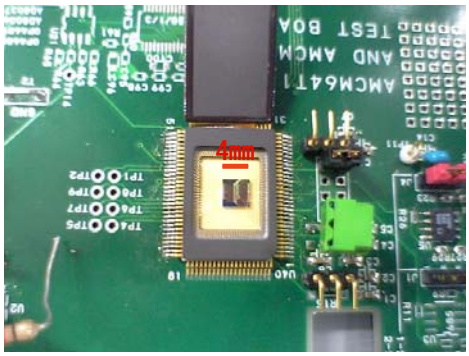

Fig. 1: Photograph of the AMC chip

II. Measurements and Results

We have developed the AMC module which consists of the AMC chip with 64 store capacitors, the pipeline ADC, and the FPGA for digital signal processing (DSP) and the data transfer by SiTCP [5] to readout the digitalized signal through TCP/IP (Figs. 3, 4). Fig. 5 shows the measurement of a linearity against an input

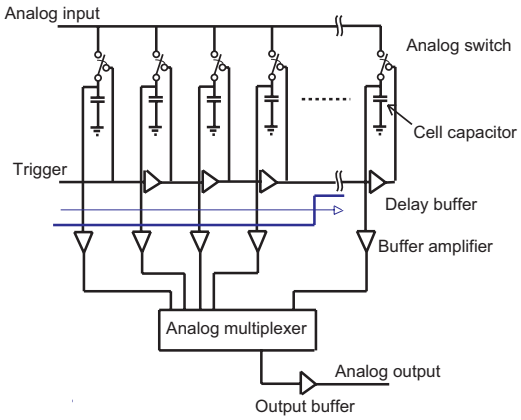

Fig. 2: Schematic view of the AMC.

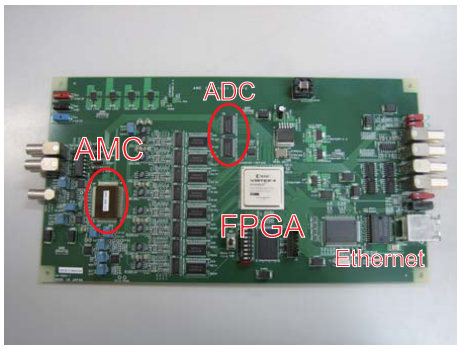

Fig. 3: AMC module

level. The AMC chip had a linearity in an input range from -0.9 V to 0.7 V with a integral non-linearity of 0.4 %. This range was limited by the back-end ADC and it can be improved to ∼2 V by optimizing this ADC. Fig. 6 shows variations of the output level against a constant input level. The noise level was 1.9 mV (RMS) and the corresponding dynamic range was 9–10 bit. The noise level was higher than ≤1.0 mV of the previous chip. It seemed that the cause is due to our modification of the capacitance of each capacitor. To improve the analog bandwidth, we changed its value from 1.0 pC to 0.2 pC. Since we can also improve the analog bandwidth by reduct the number of capacitors connecting to the input line simultaneously, this capacitance could be set to 1.0 pC and the noise level may be ≤1.0 mV. After doing these optimizations, the dynamic range would be improved to a value of ∼11 bit.

III. Summary

We have developed the AMC with 64 cells for the fast and high resolution waveform sampling of photodetectors in IACTs. The linearity, the noise level, and the dynamic range were measured. The noise level was 1.9 mV which is higher than the previous chip. This was probably due to the small capacitance of each capacitor. Based on these results, we have developed an AMC with 256 cells, optimizing parameters such as the capacitance

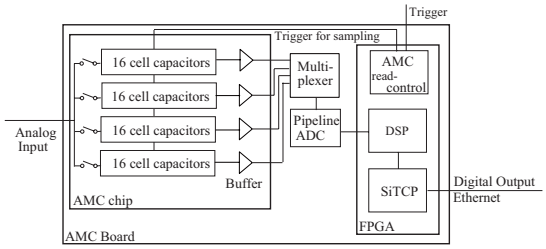

Fig. 4: Block diagram of the AMC module

of each cell. The performance of the AMC is being measured and presented in ICRC2009.

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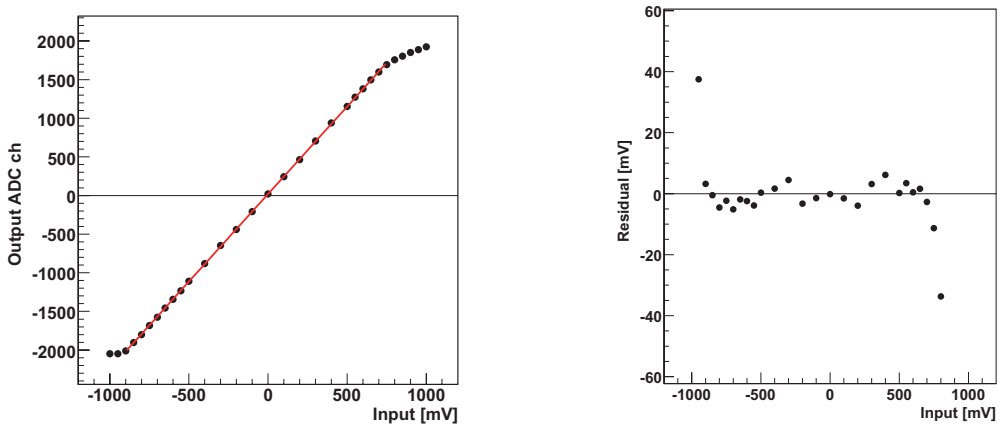

(a) Linearity (b) Residual

Fig. 5: (Left) Output values of the ADC as a function of input voltage to the AMC. Red line is a fitted line by a linear function. (Right) Residual from the fitted line.

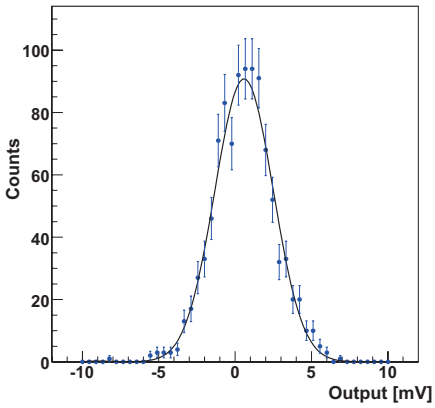

Fig. 6: Noise distribution of the AMC.