

# Data Acquisition of the JEM-EUSO project

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**Abstract.** JEM-EUSO is an observatory to investigate the origin of Ultra-High-Energy Cosmic Ray (UHECR) from International Space Station (ISS)[1]. The development of this observatory poses several challenges, including high-resolution camera with compact electronics and high speed data acquisition (DAQ) system with low power budget. JEM-EUSO electronics have to handle  $2 \times 10^5$  pixel with  $2.5 \mu\text{s}$  sampling speed with limited power budget from ISS. DAQ is based on a hierarchical architecture to reduce amount of data through a series of triggers. It is necessary to reduce data from  $\sim 640$  GB/s on the Focal Surface (FS) to  $\sim 250$  kB/s which can be down-linked on the ground. This paper describes the DAQ system of JEM-EUSO.

**Keywords:** Ultra-High Energy Cosmic Ray, Space Observation, JEM-EUSO

## I. INTRODUCTION

Observation of Extensive Air-shower from Space has been proposed since discovery of Ultra-High Energy Cosmic Rays (UHECR). The basic principle of observation is based on a calorimetric measurement of the UHECR using Fluorescence technique with huge aperture. JEM-EUSO project aims to mount a fluorescence telescope on the ISS and monitor the Earth's atmosphere. The telescope has to be capable to detect fluorescence and Cherenkov photons from the Extensive Air Showers (EAS) and to observe space-time development from 430 km altitude above sea level. Therefore, this telescope must have large aperture in small mass, high-resolution and high speed camera and DAQ electronics. JEM-EUSO has about  $2 \times 10^5$  number of pixels which will be operated with high speed sampling ( $4 \times 10^5$  Hz), high sensitivity (single photo-electron level) and low power consumptions.

The FS Electronics of JEM-EUSO consists of proximity electronics for the signal from the high resolution camera. Also it has driving circuits of the camera, LIDAR and IR camera assembly, interface between JEM-

EUSO and the ISS via the Japanese External Module (JEM) platform, Thermal control and Calibration, Direction, and Lid mechanism of the telescope.

## II. HIERARCHICAL DAQ SYSTEM

JEM-EUSO DAQ System, schematically shown in Figure 1, is designed to maximize detector observation capabilities to meet various scientific goals, to monitor system status, autonomously taking all actions to maintain optimal acquisition capabilities and handle off-nominal situation. CPU and electronics are based on hardware successfully employed in space experiments such as Pamela, Agile, Altea, Sileye-3, etc., taking into account recent developments in microprocessors and FPGA technology. Acquisition techniques and algorithms also benefit from the development performed in these missions. Radiation-Hardness technology will be employed, with ground beam tests (eg. GSI, Dubna, Himac) to qualify and test resistance of new devices. Space qualified devices will be employed wherever required by safety and agency requirements.

The DAQ system discriminates event-like signatures against various background noises based on a system trigger algorithm described in [2]. The fluorescence and Cherenkov photons coming from EAS are converted to electric charge by 36 pixel MAPMT [3]. About 5,000 PMTs, i.e.  $\sim 2 \times 10^5$  pixels, are mounted on the FS which has a curved surface of about 2.3 m in diameter. The signals from the MAPMT are digitalized by front-end ASIC [4] and FPGA for the First Level Trigger. This front-end ASICs discriminate the signals from electrical noise and the FPGAs count number of photo-electrons every  $2.5 \mu\text{s}$ . These digital data are delivered to the Second Level Trigger board. When the second level trigger is issued, data are delivered to higher hierarchy for the third level trigger which extract air-shower like events. Detail of these trigger systems are described below.

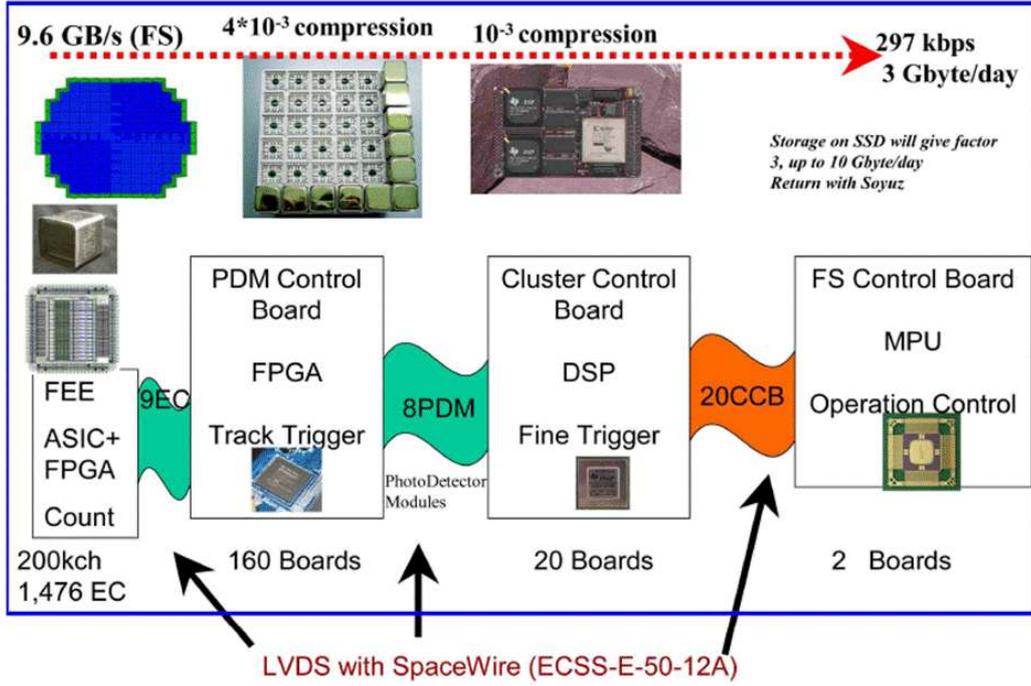


Fig. 1: Data Reduction scheme, from the Focal Surface (left), read by a Front End Electronics with an ASIC, to a PDM FPGA, a Cluster Control Board (DSP) and the main CPU (right).

#### A. First Level Trigger

First Level Trigger is issued on pixel basis: 4 MAPMTs (144 pixels), are assembled on a support structure. Signal from those pixels are delivered to the front-end ASIC [4]. In the front-end ASIC, signals greater than single photo-electron are discriminated from electrical noise. Charge (Q) of the signal is converted to time width (T) to the output pulse. The charge from single photo-electron corresponds to about 8 ns. Also Photo-electron counting method will be implemented on next version of ASIC to increase sensitivity for faint signals. The output pulse is delivered to a FPGA chip and number of photo-electrons in a GTU (Gate Time Unit =  $2.5\mu\text{s}$ ) is digitalized to 8 bits data. The digital data are labeled according to number of photo-electrons for the second level trigger. This 144 pixel block is called Elementary Cell (EC). Total data size from whole FS detector is amount of  $1.6 \times 10^6$  [bit/GTU] =  $6.4 \times 10^{11}$  [bit/s] at this trigger stage. Total power budget of ECs on whole FS is about 200 W which includes 141 W for ASICs.

#### B. Second Level Trigger

Nine ECs are packed in a Photon-Detector Module (PDM), a matrix of  $36 \times 36$  PMT pixels<sup>2</sup>. Figure 1 shows the structure of this module which is composed of 36 MAPMTs, and its assembly, PMT supports, 9 ECs, PDM board, and high voltage supply of the PMTs. 146 PDMs cover the whole FS. A dedicated FPGA chip in a PDM performs the so-called Linear Track Trigger which aims to search for correlated hits during the trigger tracking

period (11 GTUs) along predefined track angles [2].

The track trigger begins with a list of hot (active) pixels which are determined and sent by ECs every GTU. In parallel the photon counting data of every pixel (8 bit precision) are also sent multiplexed with 144 pixels from a EC. To receive all the data in a GTU, total 90 I/O lines for 9 ECs are assigned using single-ended protocol running in 100 MHz. For a given hot pixel a computation loop is taken over all 16 possible track angles. When any track angle of a hot pixel is found to have total number of hits integrated along the direction exceeding the threshold, a positive trigger decision is made. When the trigger is issued, the data in 100 GTUs around the hot pixel GTU are sent to the third level trigger. Trigger rate from whole detector on this stage is controlled to be about 1000 Hz.

The high voltage supply is designed to drive arbitrary voltage between 0 to 1000 V. Active high-voltage dividers of power saving type are used to supply high voltage to the MAPMT dynodes. The divider current is defined as 10 times larger than the anode current to bear the standard nightglow background. Also protection circuit is mounted. It protects MAPMTs from instantaneous large amount of light such as lightning. Photo-MOS relay is used to interrupt photo-electron multiplication safely.

Total power budget for the 146 PDMs is about 30 W in addition to 72 W for the high voltage supplies.

#### C. Third Level Trigger

The output data from 8 PDMs, namely about 10,000 pixels, are transmitted via dedicated Low Voltage Dif-

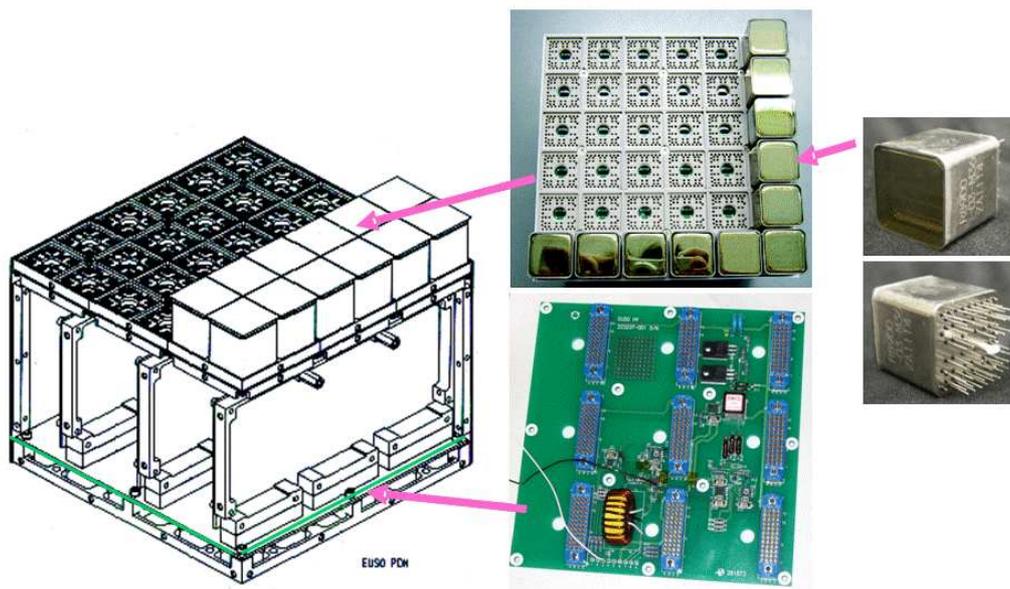


Fig. 2: PDM structure. The Focal Surface is covered with 137 PDMs. Each PDM is composed of 36 MAPMT and its support, front-end ASIC, First Level Trigger FPGA, High Voltage supply, and PDM electronics board.

ferential Signaling protocol to one of 21 Cluster Control Boards (CCB). CCB is devoted to high performance (1Gflop) trigger system to perform data reduction by three orders of magnitude. Each of the 21 CCBs performs trigger recognition on a part of the Focal Surface covered by 8 PDMs.

The fine trigger conditions are defined to extract “Air-Shower like” events on this board. Trigger rate on this stage is expected to be 0.1 Hz. Among them 1% of data will be signal from air showers.

CCBs in turn transmit pixel information which passed the fine trigger conditions via SpaceWire interfaces to the Mission Data Processor (MDP).

The losses of every part of these electronics are prohibited to be propagated to other parts so that whole functionalities are not affected.

#### D. Mission Data Processor

The CPU System (Figure 3) is composed of a number of boards devoted to different tasks including CPU main board, Mass Memory, Internal and External Housekeeping interfaces, Interfaces to ISS (1553 and Ethernet), and Fast bus interface for event acquisition. The CPU is devoted to the control of the apparatus and the general optimization of the performance of the instrument in terms of data budget and detector status. It is expected to function autonomously and to reconfigure the working parameters with little or no intervention from the ground. It will handle alarm and contingencies in real time minimizing possible damage to the instrument. Long term mission operation and observation planning from the ground will be implemented from the ground with specific telecommands, used to overrule the specific operation parameters of the instrument. By sending imme-

diately or time-delayed telecommands it will be possible to define the various operation parameters of the instrument in terms of specific physics objectives or specific situations. The CPU has a relatively low processing power (100MHz) since it is charged with the general handling of the experiment. The main CPU tasks are power on/off of all subsystems, perform periodic calibrations, start acquisition and run, define trigger mode acquisition, read Housekeeping, take care of real time contingency planning, perform periodic Download/Downlink, and handle 1553 commands.

The instrument normally stays in a waiting status or free running mode in which background noise is continuously written into the PDM ring memories. Once a third level trigger is issued, a dedicated signal runs the instrument for DAQ. The instrument continues to write data into the memories for a pre-set amount of time (exposure time). At the end of the exposure time, the instrument goes in a hold status and the read-out phase starts. During the read-out and write-out phase, the contents of the memories of the hit PDMs are downloaded into the CPU data buffer. At the end of the data download, the instrument re-starts from the waiting status to the free running mode.

#### E. Housekeeping Modules

Two different housekeeping modules are foreseen: one internal (I-HK) to the CPU system, linked via serial bus and one external (E-HK), linked to the CPU via digital line. The Housekeeping module is interfaced to the CPU with the aim to distribute command to the CPU users and to collect telemetry for monitoring purposes and optimization of observational parameters.

The internal housekeeping module is devoted to moni-

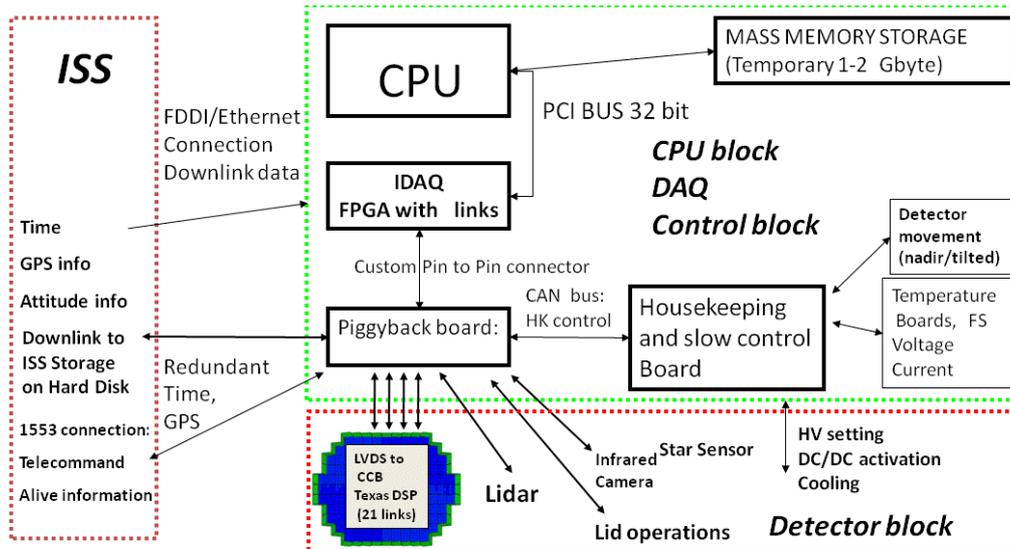


Fig. 3: Data handling block diagram, showing the detector systems (Bottom: Focal surface, Infrared Camera, thermistors...), the data acquisition and storage (Top: CPU, Mass memory...) and the ISS (left) with the relative connections.

tor of critical systems, power on/off of secondary power supply etc. I-HK is turned on together with the CPU and enables power on to all subsystems, including E-HK. Task of the latter is the general slow control and monitoring of the status of the apparatus.

I-HK functional module is capable to handle both single (upon request) or cyclic (periodic) acquisition/commanding operating mode are possible according to the acquisition program and status. Different acquisitions and controls are foreseen. For instance all relays to switch on / off secondary power supply and subsystems are controlled by High Level signals. This approach has the advantage of a great degree of flexibility keeping at the same time a strong robustness and reliability.

Some of the main electrical interfaces monitored by the module are: 1. Voltage monitor (Primary - 120V 28V; Secondary: +5V +12V , +3.3V -700V) 2. Current monitor 3. Temperature monitor 4. Contact closure (Lid status, relays) 5. Digital Communication Protocol.

#### F. Downlink / Download

Data download to ISS uses Ethernet protocol for high speed data transfer. Data are subsequently downlinked to the ground via Tracking Data Relay Satellite (TDRS) link or stored on Hard Disks. Data transmitted to the ground consists mostly of events coming from the FS but include also housekeeping information, alarms, calibration data, ancillary information, experimental data. According to available bandwidth, data are sent to the ground with highest priority given to housekeeping and alarm information. Experimental data are sent to ground with main priority to high energy events. Part of the data may be stored on board ISS on disk server. Disks are then periodically sent to the ground with Soyuz capsules.

#### G. Commands from Ground

Slow control communication from/to ground is based on MIL-STD-1553B bus. 1553 is a slow speed (1Mbit) reliable bus used in space and aeronautics for transmission / reception of critical information. In JEM-EUSO the 1553b bus is employed to:

- 1) Switch on/off the instrument or sections.
- 2) Issue telecommands from ground.
- 3) Set general acquisition parameters based on detector status. Furthermore, they can be used to patch (reprogram) part of the software at CPU, DSP or FPGA levels and dump the memory of each level in case of debugging.
- 4) Reception of keep-alive information from the detector, of nominal events, alarms.
- 5) Switch from main to spare channel (acquisition, power supply, etc.).

### III. CONCLUSION

The data acquisition and handling scheme for the JEM-EUSO project have been discussed in this paper. The DAQ is based on a hierarchical architecture designed to reduce at each level amount of data through a series of triggers controlling an increasingly growing area of the focal surface. Performance of these system have been verified based on computer simulations. The DAQ boards described in this paper are now under development, and they will be tested in laboratory in this year.

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