Front-end Readout ASIC for the JEM-EUSO Focal Surface Detector

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***Abstract*. Front-end ASIC for the focal surface of the JEM-EUSO telescope has been developed and examined. JEM-EUSO is a new type of observatory on board the International Space Station (ISS) to observe extreme energy cosmic rays. Incident photons at the telescope are detected by multi-anode photomultipliers (MAPMT) at the focal surface with 0.2 mega pixels. Photoelectrons (p.e.) at each pixel are multiplied by about 5×10^5 and the output current is fed into the front-end ASIC. Basically this ASIC converts the input electric charge Q to an output pulse with time width T which is proportional to the charge Q. Present version of the ASIC has 16 channels of analog signal inputs and Q-T converted outputs. Analog signals of each amplifier in the ASIC can be monitored. Various control circuits are implemented in the ASIC such as gain control, offset control, minimum pulse width and so on. We achieved very small power consumption 1.8 mW/channel. Linearity between Q and T, dynamic range, and other properties are described. Furthermore, to achieve a better performance new development of the front-end ASIC started using an experience of the MAROC chip.**

***Keywords*: Front-end, ASIC, DAQ, Low power**

I. INTRODUCTION

JEM-EUSO telescope [1][2][3] on board the ISS observes transient luminous phenomena in the earth's atmosphere caused by particles and waves coming from space. The telescope detects extreme energy particles with energies above about 10^{20} eV. The telescope on the ISS orbits around the earth every 90 minutes at an altitude of ∼430km. Extreme energy cosmic rays (EECR) coming to the earth's atmosphere collide with atmospheric nuclei and produce many secondary particles which form extensive air showers (EAS). JEM-EUSO captures moving tracks of fluorescent and Cherenkov UV photons produced by EAS and reproduces calorimetric development of EAS. The JEM-EUSO telescope records the tracks of EAS with a time resolution of about 1μs and an angular resolution of about 0.1°. These time-sliced images allow determining the energies and directions of the extreme energy primary particles.

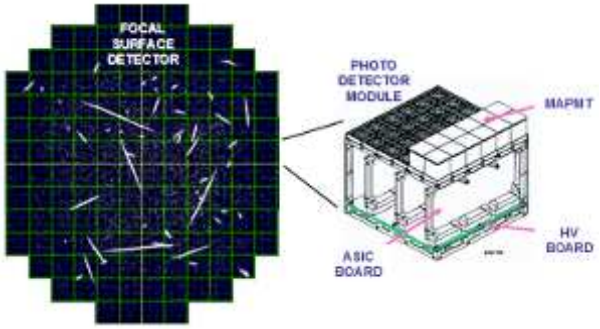

Fig. 1. Focal surface and Photo-Detector Module (PDM) of JEM-EUSO. Simulated air shower images with 10^{20} eV are shown on the focal surface. The front-end ASIC will be mounted on the ASIC board which is connected to MAPMTs.

II. FOCAL SURFACE DETECTOR AND ELECTRONICS

A conceptual figure of the focal surface of the JEM-EUSO telescope is shown in Fig.1. The focal surface is composed of 148 Photo-Detector Modules (PDM). Each PDM consists of 9 Elementary Cells (EC), each EC consists of 4 multi-anode photomultiplier tubes (MAPMT), and each MAPMT consists of 36 channels of anodes. Therefore, the focal surface is formed by more than 5,000 MAPMTs and readout electronics system consists of about 2×10^5 channels.

A conceptual block diagram of the JEM-EUSO data acquisition and trigger system is shown in Fig. 2.

Signals from the MAPMTs are fed into the front-end ASIC at which input charges are converted to pulse

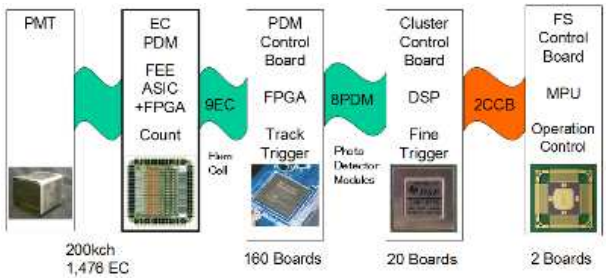

Fig. 2. Conceptual block diagram of JEM-EUSO data acquisition and trigger system.

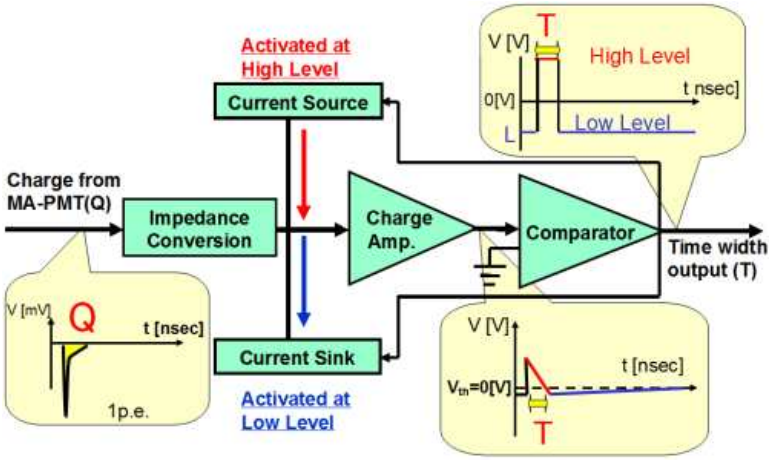

Fig. 3. Basic functional block diagram of the front-end ASIC (KI02).

widths which are proportional to the input charges. The output pulse widths and number of pulses per Gate Time Unit (GTU) are measured by Field Programmable Gate Array (FPGA), where GTU is about 1 μsec.

To trigger useful events and records them, a successive hierarchical electronics system is adopted. [4][5][6]

III. Front-end ASIC

A. Requirements

The electronics system is required to keep a high trigger efficiency with a flexible trigger algorithm as well as a reasonable linearity in the energy range of 10^{19}-10^{21} eV for EECR.

The front-end ASIC is required to count single photoelectrons (p.e.) with a double pulse resolution of 10 ns. Gain of the MAPMT is assumed to be about 5×10^5. Therefore, the charge of the single p.e. corresponds to 0.08 pC.

Noise level should be sufficiently lower than 0.04 pC to count the single p.e..

Number of photoelectrons per GTU (=2.5μs) per pixel by the fluorescent light from EAS generated by EECR with 10^{21}eV is obtained by simulations to be roughly 250 at around the shower maximum. By multiplying a safety factor of 2, it becomes 500 p.e./GTU/pixel which correspond to 40 pC/GTU/pixel.

Requirement for a power consumption less than 1-2mW/ch must be fulfilled to manage the huge number of the signal channels in an available power budget for the ASIC. Available space for the electronic circuits is very limited. Severe radiation tolerance in the space environment during scheduled operation period is required also for the system.

B. Design features

Basic functional block diagram of the front-end ASIC named KI02 is shown in Fig. 3.

MAPMT anodes are coupled in DC fashion to the input of the front-end ASIC. Current pulses are converted into voltage signals, amplified, and, then, discriminated by a built-in comparator. Input impedance of the ASIC is set to 50 Ω, which is converted to high impedance by a impedance conversion circuit. Output pulses from an amplifier are made to have triangle shapes by a current source circuit and a current sink circuit. The former works when the comparator state is high and the latter works vice versa. The output pulse width (T) from this ASIC is designed to be proportional to the input charge (Q), which is developed with a new idea for this project.

There are 14 bits of registers for each channel in the ASIC to adjust several parameters as shown in TABLE I. The pulse width, a Q-T conversion gain, and an offset for each channel are adjusted by controlling values in the registers. Test pulses to provide to all channels in the ASIC can be enabled and disabled. Output pulses from each channel can also be enabled and disabled. Each analog output from the amplifier in the ASIC can be monitored by selecting the channel.

TABLE I
Registers to adjust parameters for KI02 ASIC.

D0 D1 D2	Source current adjust
D3 D4 D5	Sink current adjust
D6 D7 D8	Charge amplification adjust
D9 D10 D11	Minimum pulse width adjust
D12	Test pulse enable
D13	Output pulse disable

C. Layout and package

Fig. 4 shows a layout figure of the front-end ASIC with a size of 3mm $\times$ 3mm. The ASIC has been designed and simulated using T-SPICE of Tanner Research

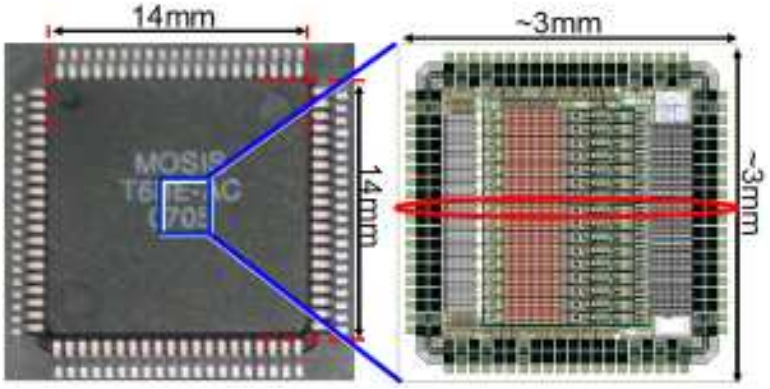

Fig. 4. 80pin QFP package (left) and a layout of KI02 ASIC (right).

Inc.. The first version of the ASIC named KI01 was made by MOSIS Integrated Circuit Fabrication Service in 2006. The second version, named KI02, was made in 2007. There are 16 channels of the above circuits in an ASIC chip. TSMC 0.25μm CMOS process is used for a fabrication of this ASIC. The ASIC chips are packed in 80pin QFP packages.

D. Test method

Various tests have been done by using a test board shown in Fig. 5. The 80pin QFP package in which the ASIC chip is packed, is directly soldered to the central part of the board. Test pulses are fed into the board from a pulse generator. PMT signals are also fed into the board after the test pulse experiment. The registers inside the ASIC were controlled by using a Linux PC via I/O board.

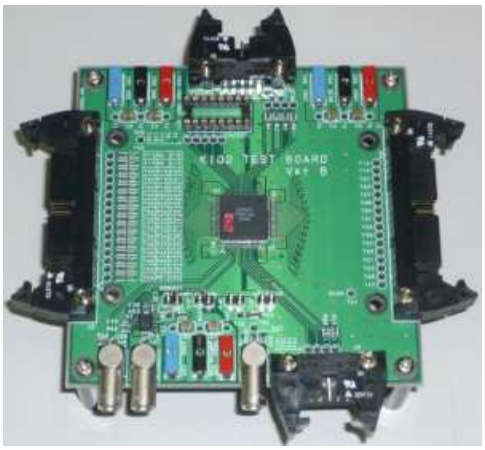

Fig. 5. Test board of the front-end ASIC KI02

E. Linearity and power consumption

Measured output pulse width as a function of input charge is shown in Fig. 6. It is shown that there is a sufficient linearity between the input charge (Q) and output pulse width (T) within a dynamic range of the input charge of 0.1-30 pC, which almost satisfies the present requirement.

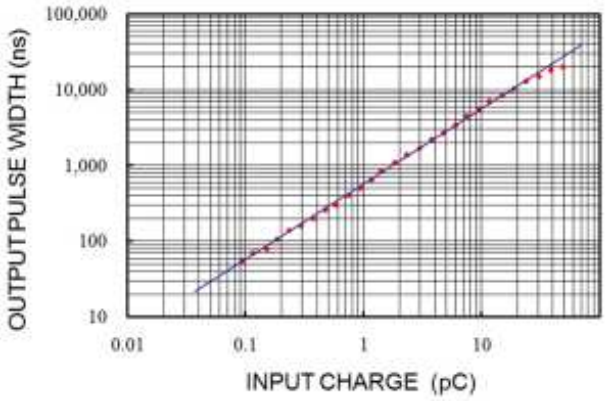

Fig. 6. Output pulse width vs. input charge.

Power consumption was measured to be 1.8 mW/channel, which is alomost consistent with the value simulated by T-SPICE.

F. PMT signal distribution

Pulse width distribution was also measured using signals from a PMT, which was illuminated by a blue LED to give roughly 20 p.e. in a short time of about 10ns. The width of the broad peak in the figure is

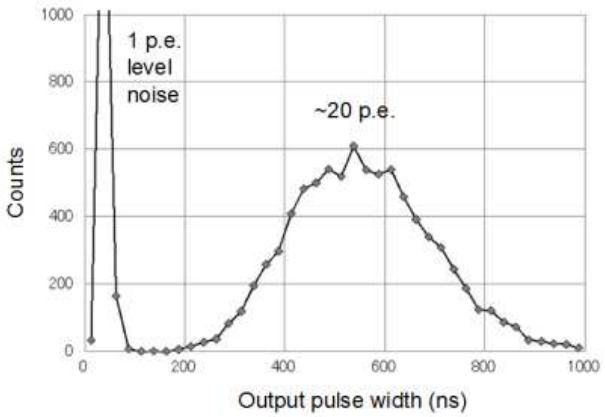

Fig. 7. Distribution of output pulse width in case PMT signals are fed into the KI02 ASIC.

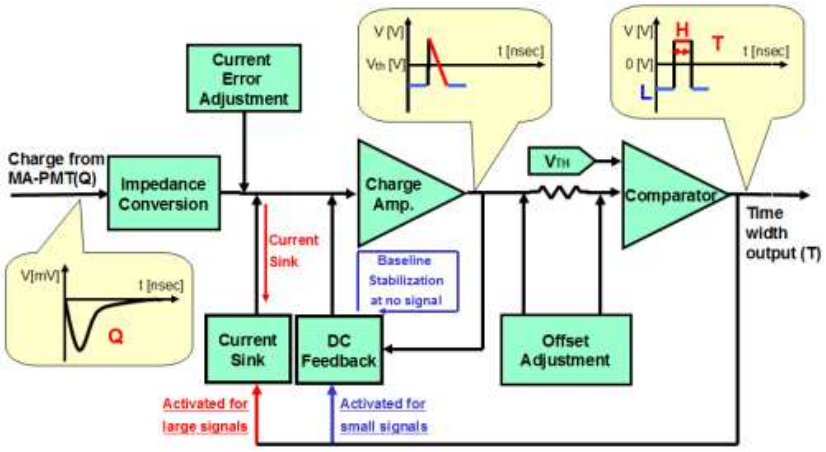

Fig. 8. Basic functional block diagram of the front-end ASIC (KI03).

roughly consistent with an error caused by the Poisson fluctuation.

IV. New Versions of the ASIC

Many improvements were applied to a circiut design to make the next version. Basic functional block diagram of the new front-end ASIC named KI03 is shown in Fig. 8.

Though the threshold voltage cannot be adjusted for the previous version KI02, it can be done for the new version KI03. The power consumption will be decreased to 0.7 mW/channel, which may be decreased till around 0.4 mW/channel by the optimization. Further noise reduction is made to the electric circuits. Detection circuits of the Single Event Upsets (SEU) caused by the radiation is newly added. The value of the supply voltages is changed for easy handling.

We are examining this new chip at present. Measured result will be shown soon.

Furthermore, to achieve a better performance new development started by a collaboration with LAL, France. New front-end ASIC will have an added basic function of real photon counting using an experience of MAROC chip [7][8]. Scalers will be added in the ASIC to reduce total power consumption. PMT gain change with optoswitches will be commanded by a logic from the ASIC.

High-density bare chip mounting board will be adopted to pack the required number of channels in the limited space.

V. Conclusions

In conclusion the front-end ASIC for the focal surface detector of the JEM-EUSO mission has been made and examined. It has been shown that fundamental functions of the ASIC work well. In the next design, the power consumption will be improved to be about 0.7 mW/ch, the noise level will be further suppressed and the handling will be much easier.

Acknowledgment

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